In the Specification

Applicant presents replacement paragraphs below indicating the changes with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

Please replace the paragraph beginning at page 2, line 21 with the amended paragraph as follows:

where Cdv is the dynamic capacitance of varicap diode Dv, which varies according to control voltage Vcom. The adjusting of the capacitance of capacitor Cv by adjustment signal FA enables adjusting the oscillator operating range. Control and adjustment circuit 8 includes ~~capacitors~~ comparators 12 and 14 enabling comparing voltage Vcom with values VH and VL. Comparators 12 and 14 control a coding block 16. Coding block 16 controls via an adder the incrementation or the decrementation of adjustment signal FA, stored in a D flip-flop 18 clocked by clock signal CKaj. The value of voltage Vcom is thus taken into account by circuit 8 at each rising edge of signal CKaj, and causes, if necessary, an immediate adjustment of the operating range.

Please replace the paragraph beginning at page 10, line 28 with the amended paragraph as follows:

Fig. 6 schematically shows a comparison circuit [[4]] 4', a filter 6, and a frequency divider 9 of a phase-locked loop including, according to the present invention, a first embodiment of a circuit 30 for inhibiting comparison circuit [[4]] 4'. For clarity, only those elements necessary to the understanding of the present invention have been shown. Circuit 30 includes a D flip-flop 31 clocked by the inverse of clock signal CKaj, and reset by clock signal CKaj. The input terminal of flip-flop 31 is connected to voltage Vdd, so that it permanently has a logic value equal to 1. The output terminal of flip-flop 31 generates an inhibition signal INH. Comparison circuit [[4]] 4' includes, in addition to the elements described in relation with Fig. 4, AND gates 34 and 35 controlled by the inverse of inhibition signal INH, respectively arranged to cancel signals UP and DWN when signal INH has a value 1.

Please replace the paragraph beginning at page 11, line 9 with the amended paragraph as follows:

Inhibition circuit 30 and signal CKaj are provided to inhibit comparison circuit [[4]] 4' and to cancel any current provided by comparison circuit [[4]] 4' to filter 6 for a given duration, called the inhibition duration, before the value of voltage Vcom is taken into account by circuit 8. Clock signal CKaj is at 0 for the inhibition duration and its switchings to 1 correspond to times when the value of voltage Vcom is desired to be taken into account. When circuit [[4]] 4' is inhibited, and no positive (respectively negative) current is provided to the filter, capacitor C2 discharges (respectively, charges) into capacitor C1 through resistor R1. The value of voltage Vcom then comes closer to the value of voltage VC1. According to the present invention, the time during which clock signal CKaj is at 0 must be sufficient for voltage Vcom to have time to substantially reach the value of voltage VC1. However, when comparison circuit 4 is inhibited, the phase-locked loop is open and it cannot converge. The time during which ~~signals~~ signal CKaj is at 0 is thus limited to reduce the time during which the phase-locked loop is open.

Please replace the paragraph beginning at page 11, line 22 with the amended paragraph as follows:

Fig. 7 schematically shows a second embodiment of an inhibition circuit 30 according to the present invention. In addition to previously-described flip-flop 31, circuit 30 includes a comparator 32 comparing value VH and the value of voltage Vcom. Circuit 30 also includes a comparator 33 comparing value VL and the value of voltage Vcom. The input terminal of flip-flop 31 receives an OR combination of the outputs of comparators 32 and 33. According to this embodiment, circuit 30 only ~~activates~~ deactivates circuit [[4]] 4' when signal CKaj is at 0 and when voltage Vcom is out of operating range VL-VH. Such an inhibition circuit 30 then enables limiting the total time during which circuit [[4]] 4' is deactivated, that is, during which the phase-locked loop remains open.

Please replace the paragraph beginning at page 12, line 14 with the amended paragraph as follows:

At a time t11, clock signal CKaj switches to 0 and comparison circuit [[4]] 4' is deactivated by inhibition circuit 30. Voltages Vcom and VC1 are substantially equal and voltage Vcom substantially does not vary.

Please replace the paragraph beginning at page 12, line 17 with the amended paragraph as follows:

At a time t12, clock signal CKaj switches to 1, and the value of voltage Vcom is taken into account by control and adjustment circuit 8. Voltage Vcom having a value greater than value VH, circuit 8 brings the oscillator into its upper operating range. Voltage Vcom still is at value V2, and the oscillator then oscillates at a frequency F3 close to maximum frequency FH1 of the oscillator in the upper operating range. The phase-locked loop then tends to bring the oscillator from frequency F3 to frequency F2. Comparison circuit [[4]] 4' and filter 6 are rapidly saturated, and control voltage Vcom is brought to a value close to ground GND, smaller than voltage VL. The oscillator then oscillates at a frequency close to minimum frequency FL1 of the upper operating range. As seen previously, capacitor C1 then discharges with a small current and voltage VC1 slowly draws near voltage Vcom.

Please replace the paragraph beginning at page 12, line 28 with the amended paragraph as follows:

At a time t13, clock signal CKaj switches to 0 and comparison circuit [[4]] 4' is deactivated. Capacitor C2 charges in capacitor C1 through resistor R1 until the value of voltage Vcom is substantially equal to the value of voltage VC1, which is greater than value VL.

Please replace the paragraph beginning at page 13, line 2 with the amended paragraph as follows:

At a time t14, clock signal CKaj switches to 1 and the value of voltage Vcom is taken into account by circuit 8. The value of voltage Vcom being included in range VL-VH, circuit 8 does not adjust the operating range of the oscillator. After time t14, comparison circuit [[4]] 4' is

reactivated and the phase-locked loop operates again. The phase-locked loop brings voltage Vcom back to a value close to value GND before bringing it to its expected value V4 in a damped sinusoid.

In the Drawings

A Request for Corrections, Approval and Entry of Drawings is enclosed.

Figure 7 has been amended to correct a minor error in the drawing. Specifically, the inverting and non-inverting inputs of comparator 32 have been changed to provide consistency between the figure and the written description.

Applicants present 1 replacement sheet and 1 annotated sheet showing the amended changes.